Abstract

A BISR scheme which provides for on-chip assessment of the amount of repair on a given memory and for the flagging of any device as a fail when the device exceeds a pre-determined limit. Preferably, a counter is built and loaded through a test pattern during production testing, and the counter establishes the threshold for pass/fail criteria. The BISR is configured to load a repair solution and then test the memories for any additional failures and if there are any, repair them (provided enough redundant elements are available). In addition, a reliability controller for BISR designs can be provided, where the reliability controller contains a register set and a number of counters at the chip-level which can be loaded through a test pattern during production tests, where one of the counters contains the number of memories to be allowed for repair.